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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/420,086	10/18/99	FARNWORTH W	98-0105.01

MM92/0108

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EXAMINER	
PAREKH, N	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademark

Office Action Summary

Application No.	Applicant(s)
09/420,086	Farnworth et al
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Dec 14, 1901*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *25-46* is/are pending in the applicat

Of the above, claim(s) *40-46* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *25-39* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *5, 6*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461) in view of Pedder (US Pat. 5717245).

Regarding claim 25, Hembree discloses a semiconductor component/package comprising:

- a composite substrate/interconnect (14/16 in Fig. 2) comprising a first surface with a conductive layer/trace (40, 56, 58, etc. in Fig. 2 and 4) and second surface (31 in Fig. 2)
- a plurality of conductors on the first surface (Fig. 4 and 5; Col. 6, line 21), each conductor comprising grooves/raised contact members (40 and 66/68 in Fig. 2) through the conductive layer and configured for electrical connection with the semiconductor die
- a plurality of conductive lines/vias in the substrate/interconnect (49 in Fig. 3A) in electrical communication with the conductors (40 in Fig. 2), and
- a plurality of external contacts on the second surface in electrical communication with the conductive vias (38 in Fig. 2; Col. 4, line 53)

(Fig. 2-5A; Col. 3, line 45- Col. 6, line 65).

Hembree fails to specify using laser machined grooves formed through the conductive layer. Pedder taches using conductive stubs/grooves formed/trimmed by conventional laser trimming (Col. 2, line 25, Col. 8, line 38; Fig.2, and 9) on the conductive layer/trace of the substrate in a multichip module/ball grid package. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate laser machined grooves formed the conductive layer to improve the electrical performance of the contacts/device using Pedder's conductor layout in Hembree's component as cited in claim 25.

Regarding claims 26 and 27, Hembree discloses a semiconductor die flip chip mounted to the conductors/substrate but fail to specify using a plurality of dice flip chip mounted or wire bonded to the conductors. Pedder taches using a multichip module/ball grid package where the a semiconductor chip or multichip can be mounted on the conductors using conventional wire bond or flip chip connections (Fig. 2; Col. 2, line 36; Col. 4, line 28; Col. 4, line 50). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate a plurality of dice flip chip mounted or wire bonded to the conductors to achieve multichip connection capability using Pedder's module design in Hembree's component as cited in claims 26 and 27.

Regarding claim 28, Hembree discloses a the substrate comprising a material selected from the class consisting of plastic, glass filled resin, silicon and ceramic (Col. 2, line 17-33; Col. 6, line 35).

Regarding claim 29, Hembree discloses external contacts comprising balls in a ball grid array (Fig. 2-3A; Col. 4, line 48).

Regarding claims 30-32, Hembree discloses a semiconductor component/package comprising:

- a composite substrate/interconnect (14/16 in Fig. 2) comprising a surface with a conductive layer/traces (40, 56 and 58 in Fig. 2 and 4) having a thickness
- a plurality of conductors having width and thickness (40, 56, 58 and 60 in Fig. 2, 4 and 5) on the first surface (Fig. 4 and 5; Col. 6, line 21), each conductor comprising grooves/raised contact members (40, 58, 60, 66, 68, etc. in Fig. 2, 4 and 5) through the conductive layer (Fig. 2-5A; Col. 3, line 45- Col. 6, line 65), the conductor including a plurality of first pads (60 in Fig. 4-5A)
- a semiconductor die mounted on the substrate, the die comprising a plurality of second pads bonded (62 in Fig. 5A) to the first pads (Col. 6, line 25)
- a plurality of conductive lines/vias in the substrate/interconnect (49 in Fig. 3A) in electrical communication with the conductors (40 in Fig. 2), and

- a plurality of external contacts on the second surface in electrical communication with the conductive vias (38 in Fig. 2; Col. 4, line 53)

(Fig. 2-5A; Col. 3, line 45- Col. 6, line 65).

Hembree fails to specify using laser machined grooves formed through the conductive layer where the conductors include a first and second conductors configured in communication with signal and ground/voltage path respectively and having the thickness of the conductive layer and width of the grooves selected to provide an impedance value for the first conductor. Pedder taches using conductor/trace wiring design where the conventional wiring layout parameters such as spacing, pitch, number of conductors, vias, etc. are selected to achieve the desired electrical performance related to electrical signal, power/ground, impedance and frequency requirements (Col. 5, line 11- Col. 6, line 50) for the multichip module/package. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate laser machined grooves formed through the conductive layer where the conductors include a first and second conductors configured in communication with signal and ground/voltage path respectively and having the thickness of the conductive layer and width of the grooves selected to provide an impedance value for the first conductor to achieve the design and performance requirements using Pedder's wiring design in Hembree's component as cited in claims 30-32.

Claim 33 is rejected as explained above for claims 30 and 25-27.

Regarding claim 34, Hembree fails to specify using an encapsulant covering the die and a portion of the surface. Peddler teaches using the conventional sealant/encapsulant to encapsulate the BGA package/module in the chip packaging art (Col. 1, line 55). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to use an encapsulant covering the die and a portion of the surface to provide added protection in Hembree's component as cited in claim 34.

The combined teachings of Hembree and Pedder as explained above for claims 30 and 25 apply to claims 35 and 37.

Claim 36 is rejected as explained above for claims 35 and 34.

Claims 38 and 39 are rejected as explained above for claims 35, 25 and 28.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-05-00

Tom Thomas